NEW ASPECTS CONCERNING THE BIAS AND TEMPERATURE DEPENDENCE OF INTRINSIC NOISE GENERATORS IN EXTRACTED FET MODELS

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ABSTRACT

A systematic experimental investigation of FET noise models illustrates bias and temperature dependencies that help to explain differences between two prevalent models. Observations concerning the bias dependence of the popular temperature based noise model show that the gate noise temperature follows the ambient temperature only near the minimum noise bias condition.

INTRODUCTION

The further development and understanding of CAD models for temperature dependent simulation of active devices is critical for circuit design in commercial applications which may not have the luxury of stabilized ambient environments. To do this, a large amount of bias and temperature dependent data has been collected to develop models that account for both bias and temperature variation, for example [1]. Either of two prevalent noise models [2] or [3] can be used to extract a table of model coefficients necessary to simulate bias and temperature dependencies. Subsequently, it is of technical interest to compare the resulting variations of the model coefficients with respect to how the intrinsic FET noise is interpreted. In this work, assumptions about the FET gate noise and drain noise generators are studied for several FET technologies, of which extensive CAD modeling effort has been given. These include GaAs based MESFETs and PHEMTs and an InP based HEMT. The bias dependence of the noise model coefficients, particularly T_{gate} and T_{drain}, are investigated here. The resulting observations suggest why differences have been reported between the FET noise models of Pucel et. al.[1] and Pospieszalski[3].

Extraction procedures for temperature dependent FET noise modeling at microwave frequencies have been described and applied to several FET technologies [4],[5]. Figures. 1 and 2 show the intrinsic noise models along with their associated parasitic networks, which contribute thermal noise only.

This work reflects the results of two laboratories, and the model variations versus temperature of several unrelated FET types from several foundries. The variables of interest include the bias potentials, the ambient temperature and the material composition of the FET channel. The most recent studies of the bias variation of these noise model coefficients are[6],[7]. In [7], T_g was assumed to be constant and temperature variations of the noise coefficients were not considered. This leads to the following questions: 1) What are the bias dependencies of the noise temperature model coefficients for differing FET types and does the interpretation of gate noise subsequently change? 2) What is the resulting effect upon the drain noise temperature due to question (1). 3) What range of thermally induced variation occurs on the noise model coefficients versus bias?

RESULTS

Bias Dependence

The intrinsic noise of the FET has two interpretations according to the two models discussed above. For the PRC model gate noise is the result of random variation of physical factors such as the

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depletion layer boundary or the density of the 2DEG, and a correlated component of drain noise. In the noise temperature model the gate noise is found to be purely thermal noise, as evidenced by a linear tracking of the coefficient T_g versus the ambient temperature [3]. No correlated component of drain noise is assumed. Therefore, at room temperature, one possible assumption according to [3] is for $T_g=T_o=300K$. Extracted results for this work from several FET types are shown in Fig. 3. The noise temperature T_g is shown to have a gate bias dependence as reported in [6]. The extracted values of T_g in Fig. 3 indicate minima that are correspondingly associated with low noise bias conditions for the devices described. Although these values of T_g may be lowered (due to uncertainty in the resistance R_i) to correspond with the assumption of purely thermal noise, the bias dependence of T_g suggests that additional noise mechanisms need to be accounted for. Leakage currents from gate to drain and gate to source were found to be significant only in the case of the double δ-doped PHEMT. Otherwise, the inclusion of a correlated drain noise component with increasing current levels does correspond well to the observed bias dependence of the factor C in the PRC model. For example, the magnitude of C increases from 0.24 to 0.94 over the range $-1.0V \le V_{gs} \le -0.2V$ for the FET B1 of Fig. 3. In the case of FET A1, the magnitude of C is 0.7 for a range of bias where T_g is correspondingly flat, and the magnitude of C increases to greater than 1.0 for $V_{gs} \le -0.8$ V and $V_{gs} \ge -0.4$V corresponding to the increase of T_g for FET A1 in Fig. 3. Further data concerning the partial correlation of drain noise to the gate is discussed below with regard to the observed temperature variations.

Effects Upon Drain Noise

The second observation from Fig. 3 is that the variation of T_g versus bias is up to five times less than that observed for T_d, as shown in Fig. 4. Therefore, for a FET with a particularly broad low- noise gate bias response, such as FET A1 in Fig. 3, the assumption of only thermal noise may not severely limit subsequent interpretations of the drain noise temperature T_d. This is shown for the extracted values of T_d for FET A1 in Fig. 4. These correspond well with the T_d values for FETs studied in [7], which assumed $T_g=T_{ambient}$ versus drain current level. However, for FETs B1 and B2 the use of the extracted values of T_g given in Fig. 3 results in T_d values that remain lower for higher current levels than observed in [7]. Still, these values of T_d eventually become too high (T_d>5400K) to be considered as temperatures related to distinct physical processes in the FET channel, as noted by [7] and [8].

Temperature Dependence

Following the description of thermal coefficients used in [4], [5] and [8] the temperature dependence of the model parameters is modeled by the linear relation:

$$P(T) = P(T_o) \cdot (1 + \beta\,(T - T_o)) \qquad (1)$$

where $P(T)$ is the ambient parameter value, $P(T_o)$ is the nominal parameter value and β is the thermal coefficient of the parameter of interest. The linear variation of T_g described in [3] over temperature would correspond to a thermal coefficient, β_{Tg} ,equal to 3.33×10^{-3} /°C. This is shown as a constant, dotted line, in Fig. 5. Observations for FETs from several foundries (listed as A, B or C) measured at separate laboratories (Lab 1 measuring A and B, Lab 2 measuring C) are also shown in Fig. 5. The measured temperature range for data on FETs from A and B was 25 °C≤T≤100 °C while the range for FETs from C was -60 °C≤T≤140 °C. These independently extracted results show $6.0\ (10^{-3}/°C) < \beta_{Tg} < 20.0\ (10^{-3}/°C)$. These thermal coefficients are also observed to have a gate bias dependence for both the MESFET and HEMT technologies. To understand this requires consideration of the equivalence between the gate noise for the two models given by(2a)[3]:

$$T_g = \frac{R}{g_m R_i} \cdot T_o \qquad \text{(a)}$$

$$T_d = P\,\frac{g_m}{g_{ds}} \cdot T_o \qquad \text{(b)} \qquad (2)$$

the fact that T_g does not vary linearly as T/T_o in Fig. 5 can be accounted for by the differences in the variation of the transconductance, g_m , and the channel resistance, R_i. In the results for Fig. 5 the variation of R_i for the PHEMT, B1, is small compared to the change in g_m which has a negative β coefficient that increases with increasing current levels as g_m saturates.

The result is that FET B1 shows the largest thermal variation of the gate noise temperature T_g. Smaller changes in T_g versus temperature are observed for FETs A1 and C1 as the thermal coefficients of R_i and g_m are more similar and effectively cancel out. As noted in [7], effects of this type should not be unexpected, as the factors in (2) depend upon physical quantities like depletion widths and carrier velocities that are themselves temperature dependent.

Regarding the possible partial correlation of drain noise to the gate, the observed temperature coefficients (β_{Tg}, β_{Td}) for T_g and T_d should be about the same. This trend is seen in the values for β_{Tg} and β_{Td} shown in Figs. 5 and 6. Exact agreement is not expected since only partially correlated drain noise was observed, and additional factors in (2b) concerning the variation of T_d must ultimately be considered.

CONCLUSIONS

A bias and temperature dependent study of the intrinsic noise model generators associated with two prevalent FET noise models has been conducted. The significance of this work lies in the wide variation of bias, temperature and FET types that are considered. This consideration of a broad range of factors provides evidence as to why the two models studied may reveal differing interpretations of FET noise based upon bias condition and material composition.

Results show that the bias dependence of the correlation between the noise generating mechanisms in the FET channel can explain the observed model differences for gate noise. Gate noise temperature that increases faster than the ambient temperature change is also reported here by two independent laboratories. These variations were explained in part by the need to consider the thermal variations of the small signal model elements g_m and R_i, which are also bias and temperature dependent.

Results given here show that whether $T_g = T_{ambient}$ is assumed or not similar results for T_d values are found when the FET has a broad low-noise gate bias dependence. In general, this study shows that lower T_d values are observed for higher current levels when a gate noise process with greater than a purely thermal noise characteristic is used. However, the drain noise temperature still exceeds values expected from physically based Monte Carlo simulations of FET channel noise.

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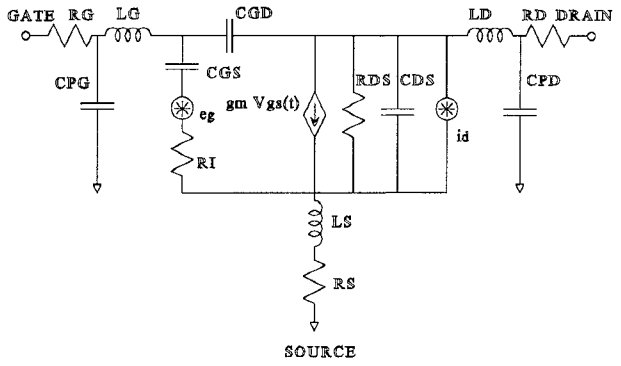

Figure 1 Small signal and noise model given by [1], where $|e_g|^2=4kT_oR/gm$ and $|i_d|^2=4kT_oP$ gm.

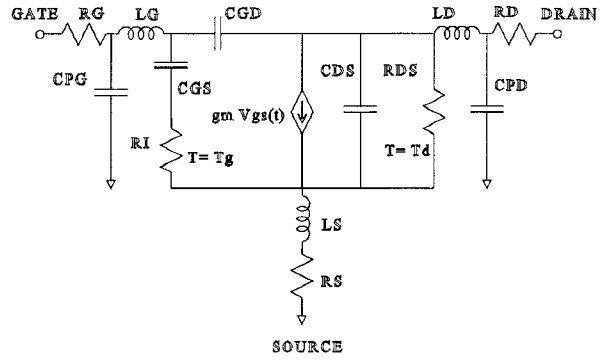

Figure 2 Small signal and noise model given by [2], where T_g and T_d are the noise temperatures of R_i and R_{ds} respectively.

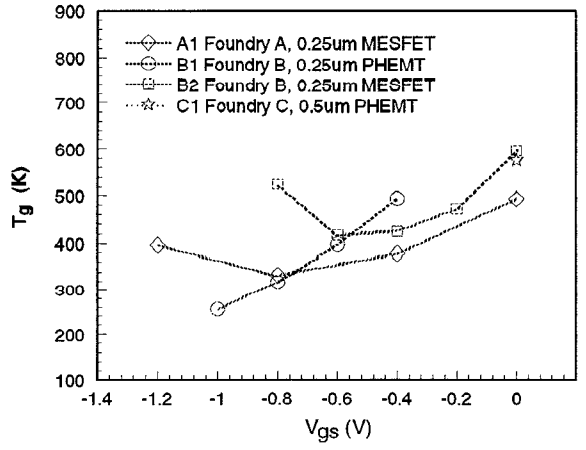

Figure 3 Extracted variation of T_g (K) versus V_{gs} (V) at T_o=300K for several FET types.

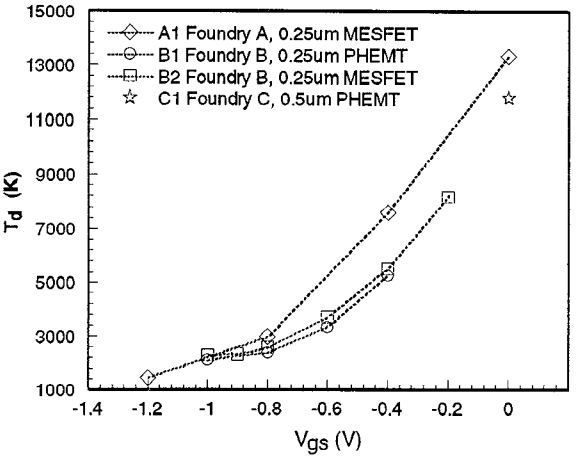

Figure 4 Extracted variation of T_d (K) versus V_{gs} (V) at T_o=300K for several FET types.

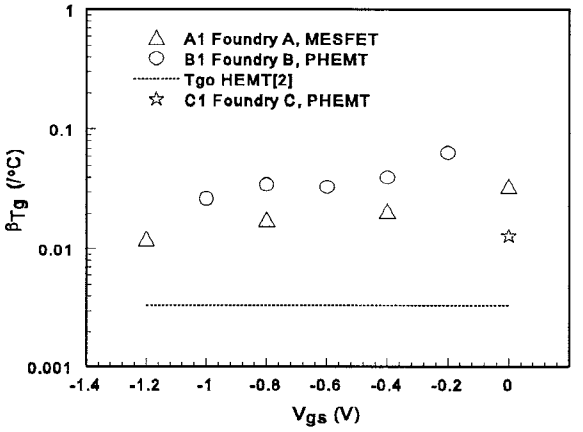

Figure 5 Comparison of extracted thermal coefficients for T_g versus V_{gs} for several FET types and the variation given by [2] (dotted).

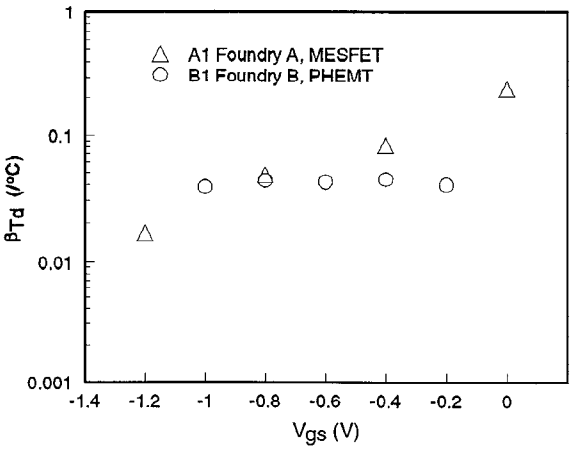

Figure 6 Comparison of extracted thermal coefficients for T_d versus V_{gs} for two FETs.